

**Introduction**

The ISL8107 is a single-phase PWM controller that operates from 9V to 75V bias supply voltage. The PWM controller drives an external high-side N-Channel MOSFET in a non-synchronous buck converter topology. The ISL8107 features input voltage feed-forward compensation and overcurrent protection, etc. For a more detailed description of the ISL8107 functionality, refer to the ISL8107 Data Sheet <http://www.intersil.com/data/fn/fn6605.pdf>.

**The ISL8107EVAL2Z Reference Design**

The ISL8107EVAL2Z evaluation board is designed to meet the output voltage and current specifications shown in Table 1. Schematic, bill of materials, and layout plots are included.

**TABLE 1. ISL8107EVAL2Z DESIGN PARAMETERS**

PARAMETER	MIN	TYP	MAX
Input Voltage (V <sub>IN</sub> )	18V	48V	75V
Output Voltage (V <sub>OUT</sub> )		12V	
Output Voltage Ripple		30mV	
Continuous Load Current			5A
Switching Frequency		200kHz	

**Quick Start Evaluation**

Figure 1 shows a photograph of the ISL8107EVAL2Z board.



**FIGURE 1. ISL8107EVAL2Z**

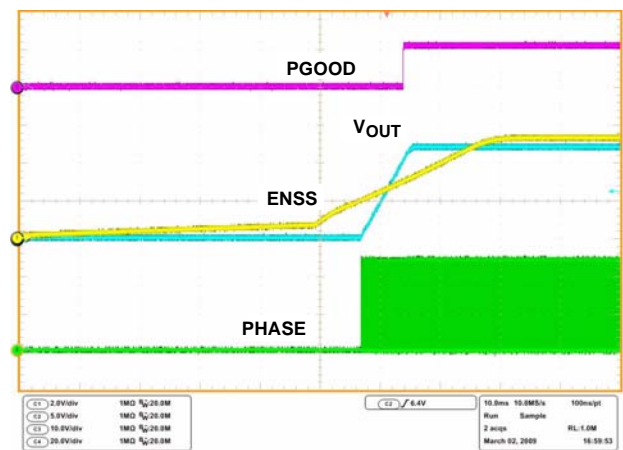
**Circuit Setup**

The input supply of the power stage can be connected to the terminals P5 (V<sub>IN</sub>) and P6 (PGND). For single supply application, the ISL8107's bias supply can be tied to V<sub>IN</sub> through J1 with shunt between pins 2 and 3. When using separate supplies, provide the ISL8107 bias voltage through P1 (VBIAS) with J1's shunt between pins 1 and 2. The load can be connected to terminal P7 (V<sub>OUT</sub>) and P8 (PGND). TP3 and TP4 can be used for DMM to measure the output voltage. Enabling and disabling the controller can be done through the toggle switch, SW1.

**ISL8107EVAL2Z Performance**

**Start-Up**

Figure 2 shows the start-up waveforms of the ISL8107EVAL2Z. Upon the VCC and VFF exceeding their rising POR thresholds, the ISL8107 provides initially 2μA to charge the soft-start capacitor, C<sub>SS</sub>, connected to the ENSS pin. If the voltage at this pin is allowed to rise (the toggle switch, SW1, at ON position), the voltage on ENSS pin will ramp-up with at a slope determined by the 2μA current and the value of the soft-start capacitor. When the voltage at ENSS reaches 0.77V, the oscillator circuit is active, and generates sawtooth waveform. At the same time, the soft-start current is increased to 33μA; the ENSS voltage then ramps up at a faster rate. The UGATE starts switching when the ENSS voltage reaches 1.4V (Typ).



**FIGURE 2. START-UP WAVEFORMS**

**Output Voltage Ripple**

Figure 3 shows the ripple voltage on the output of the regulator at 5A load current.

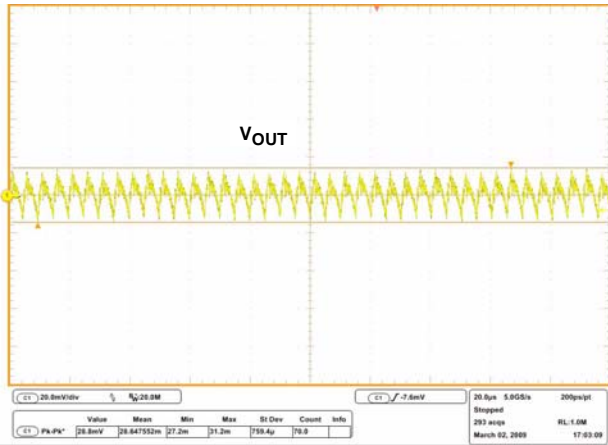


FIGURE 3. OUTPUT VOLTAGE RIPPLE @ I<sub>OUT</sub> = 5A

**Transient Responses**

Figures 4, 5, and 6 show the response of the output when subjected to transient loading from 1A to 5A at 1A/μs (within continuous conduction mode).

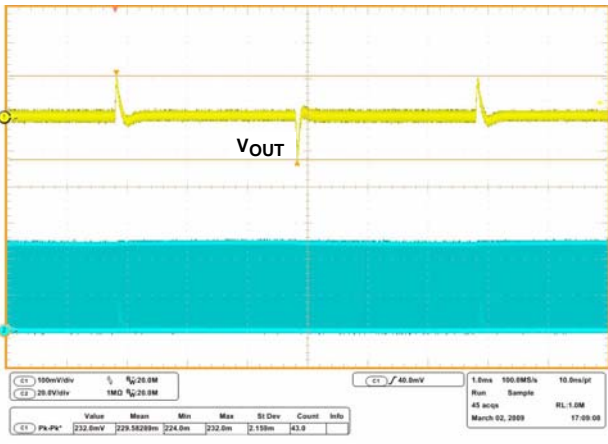


FIGURE 4. OUTPUT TRANSIENT

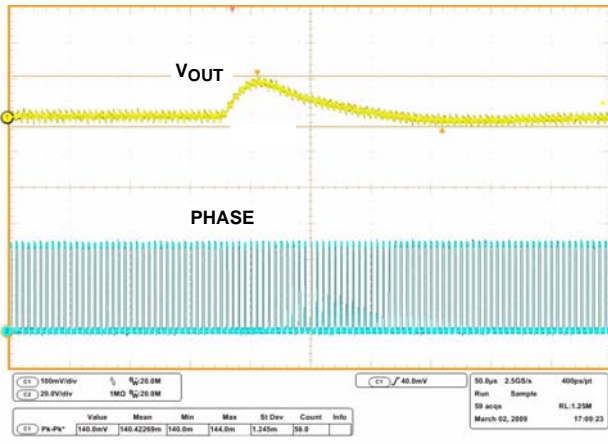


FIGURE 5. OUTPUT TRANSIENT

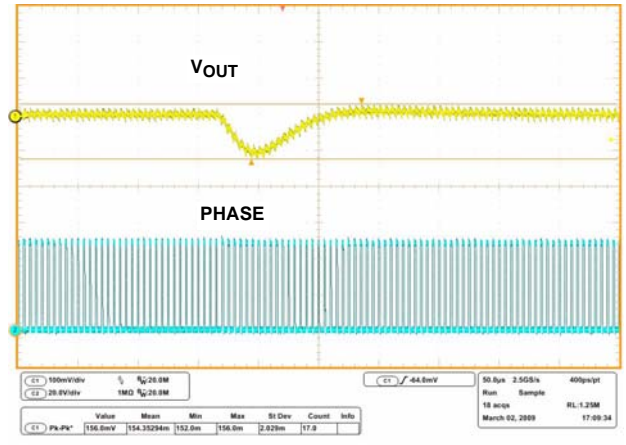


FIGURE 6. OUTPUT TRANSIENT

Figure 7 shows the response of the output when subjected to transient loading from 0.1A to 5A at 1A/μs (transition between continuous conduction mode and discontinuous conduction mode).

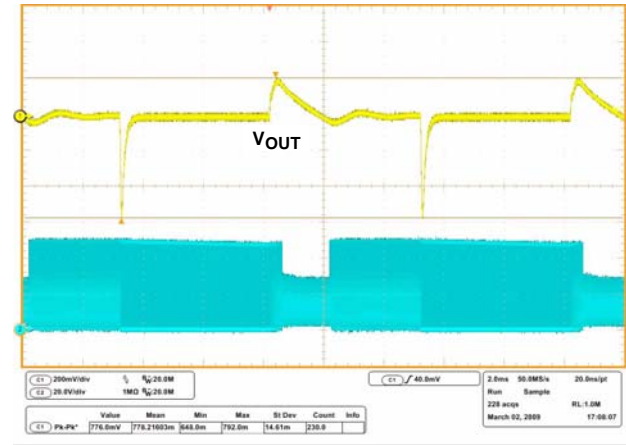


FIGURE 7. OUTPUT TRANSIENT

**Efficiency and Line Regulation**

The efficiency and the line regulation of the evaluation board with various input voltages are shown in Figures 8 and 9, respectively.

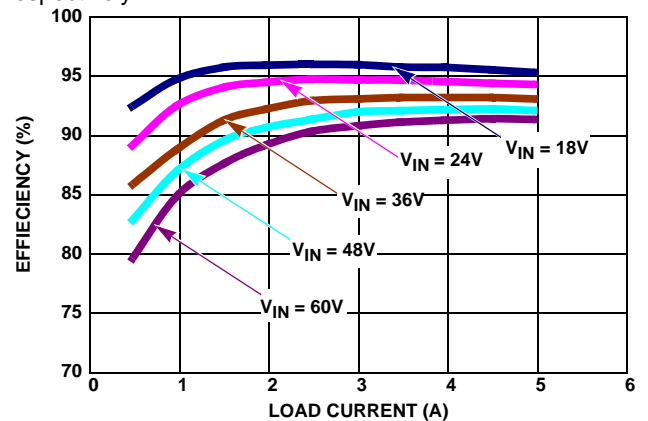


FIGURE 8. CONVERTER EFFICIENCY (V<sub>OUT</sub> = 12V)

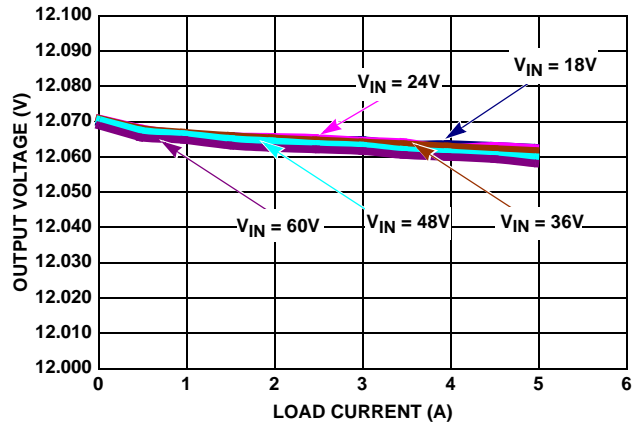
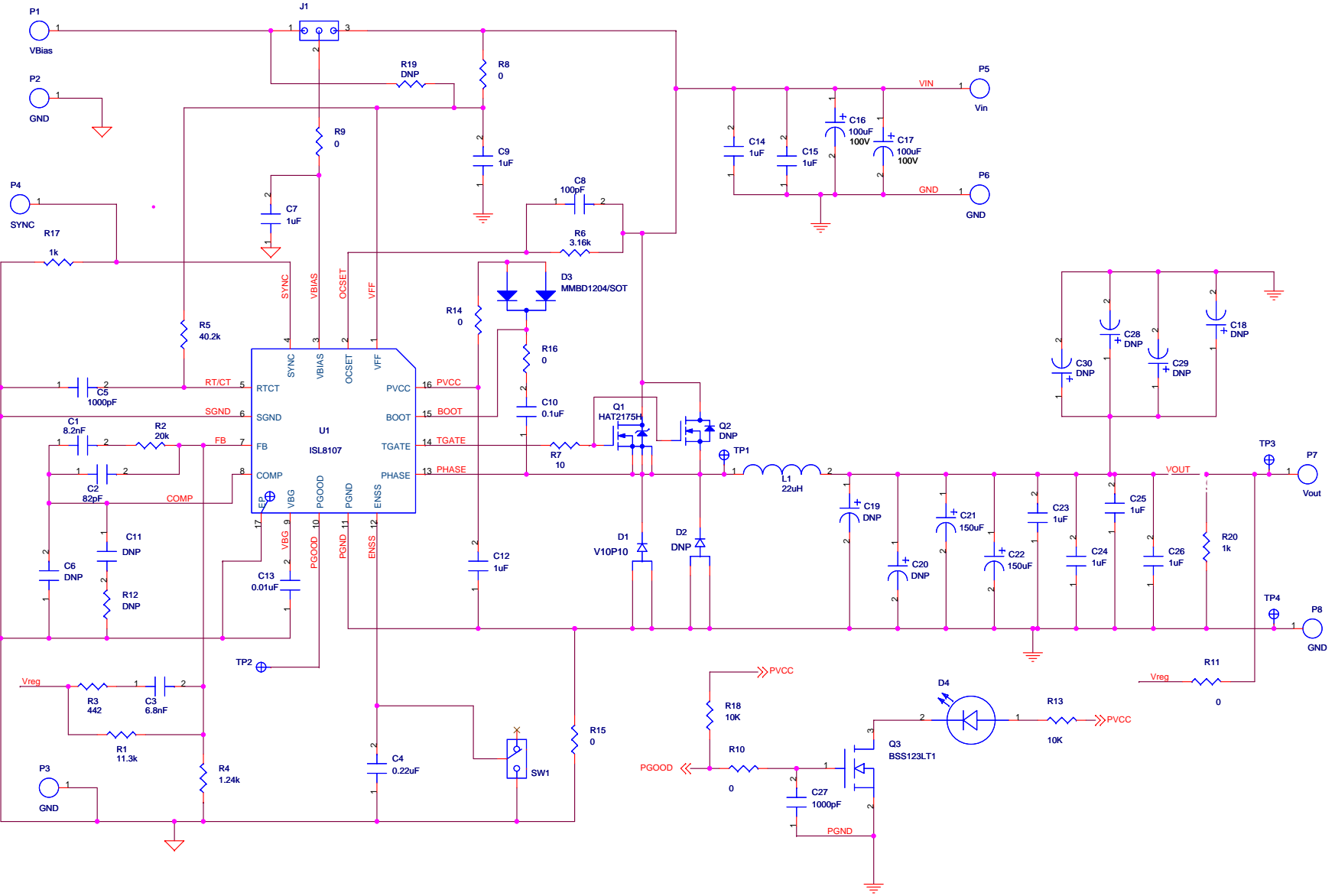


FIGURE 9. LINE REGULATION FOR  $V_{OUT} = 12V$

# ISL8107EVAL2Z Schematic



## Application Note 1459

### Bill of Materials

REFERENCE	QTY	PART NUMBER	DESCRIPTION	PACKAGE	VENDOR
U1	1	ISL8107IRZ	Single PWM Controller	16 Ld QFN	Intersil
Q1	1	HAT2175	100V N-Channel MOSFET	LFPAK	Renesas
Q3	1	BSS123LT1G	N-Channel MOSFET, 0.17A	SOT-23	On Semi.
D1	1	V10P10	100V Schottky Diode Rectifier	TO-277A	Vishay
D3	1	MMBD1204	100V Ultrafast Diode	SOT-23	Fairchild
D4	1	597-3311	LED Green	SMD1206	DIALIGHT
L1	1	HC9-220-R	22 $\mu$ H Power Inductor	SMD 12.9x13.2	Coiltronics
Q2, D2	0	DNP			
<b>CAPACITORS</b>					
C1	1		8200pF, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C2	1		82pF, 50V, COG, 10%, Ceramic Capacitor	0603	Various
C3	1		6800pF, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C4	1		0.22 $\mu$ F, 16V, X7R, 10%, Ceramic Capacitor	0603	Various
C5	1	GRM2195C2A102JA01D	1000pF, 100V, COG, 5%, Ceramic Capacitor	0805	Murata
C7, C9, C14, C15	4		1 $\mu$ F, 100V, X7R, 10%, Ceramic Capacitor	1210	Various
C8	1		100pF, 50V, COG, 10%, Ceramic Capacitor	0603	Various
C10	1		0.1 $\mu$ F, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C12, C23, C24, C25, C26	5		1 $\mu$ F, 25V, X5R, 10%, Ceramic Capacitor	0805	Various
C13	1		0.01 $\mu$ F, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C16, C17	2	100ME100PX	100 $\mu$ F, 100V, Aluminum Electrolytic Capacitor	RAD 12.5x20	Sanyo
C21, C22	2	20SEQP150M	150 $\mu$ F, 20V, OSCON Capacitor	RAD 10x13	Sanyo
C27	1		1000pF, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C6, C11, C18, C19, C20, C28, C29, C30	0	DNP			
<b>RESISTORS</b>					
R1	1		Resistor, 11.3k $\Omega$ , 1%, 1/10W	0603	Various
R2	1		Resistor, 20k $\Omega$ , 1%, 1/10W	0603	Various
R3	1		Resistor, 442 $\Omega$ , 1%, 1/10W	0603	Various
R4	1		Resistor, 1.24k $\Omega$ , 1%, 1/10W	0603	Various
R5	1		Resistor, 40.2k $\Omega$ , 1%, 1/10W	0603	Various
R6	1		Resistor, 3.16k $\Omega$ , 1%, 1/10W	0603	Various
R7	1		Resistor, 10 $\Omega$ , 1%, 1/10W	0603	Various
R8, R9, R10, R11, R14, R15, R16	7		0 $\Omega$ Resistor, 1/10W	0603	Various
R13, R18	2		Resistor, 10k $\Omega$ , 5%, 1/10W	0603	Various
R17	1		Resistor, 1k $\Omega$ , 1%, 1/10W	0603	Various
R20	1		Resistor, 1k $\Omega$ , 1%, 1W	2512	Various
R12, R19	0	DNP			
<b>OTHERS</b>					
J1	1	68000-236-1X3	Connector Header		BERG/FCI
SW1	1	GT11MSCKE	SMD Toggle Switch		C&K
P1 through P8	8	1514-2	Turret Post		Keystone

ISL8107EVAL2Z Layout

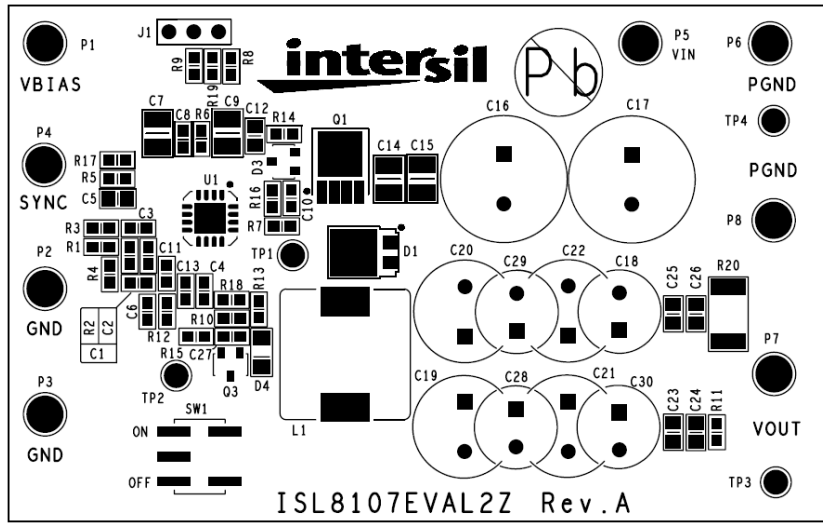


FIGURE 10. TOP SILK SCREEN

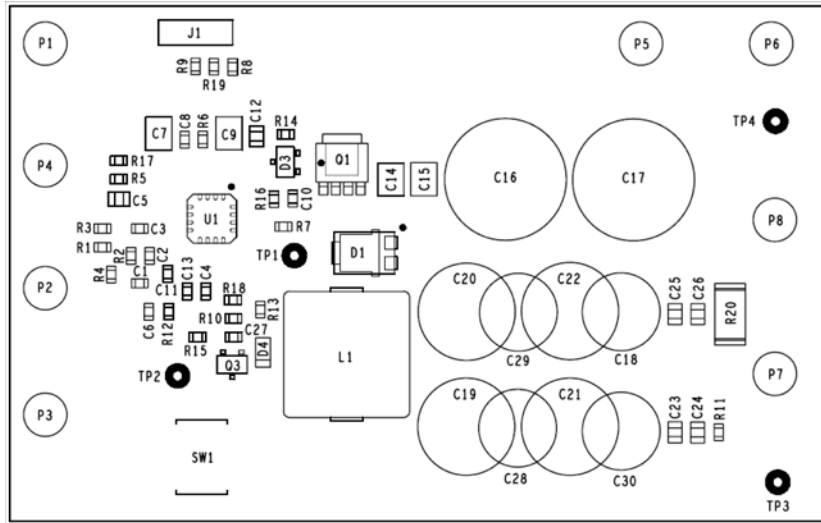


FIGURE 11. TOP ASSEMBLY

ISL8107EVAL2Z Layout (Continued)

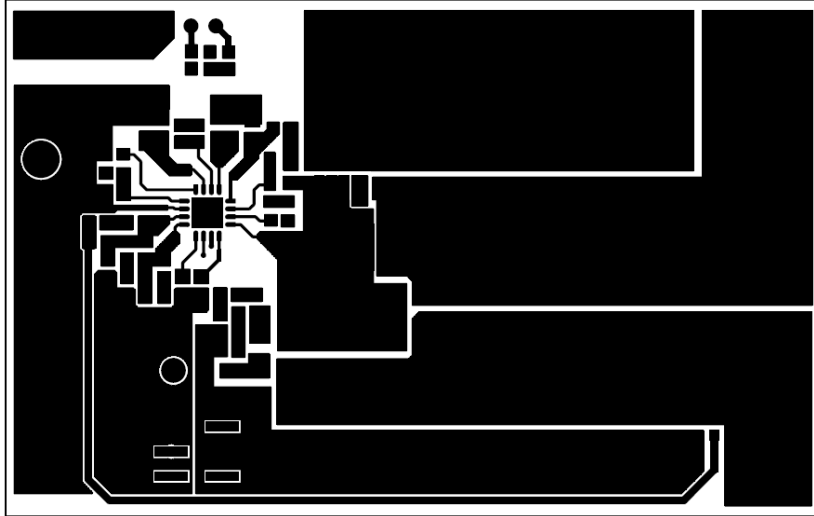


FIGURE 12. TOP LAYER

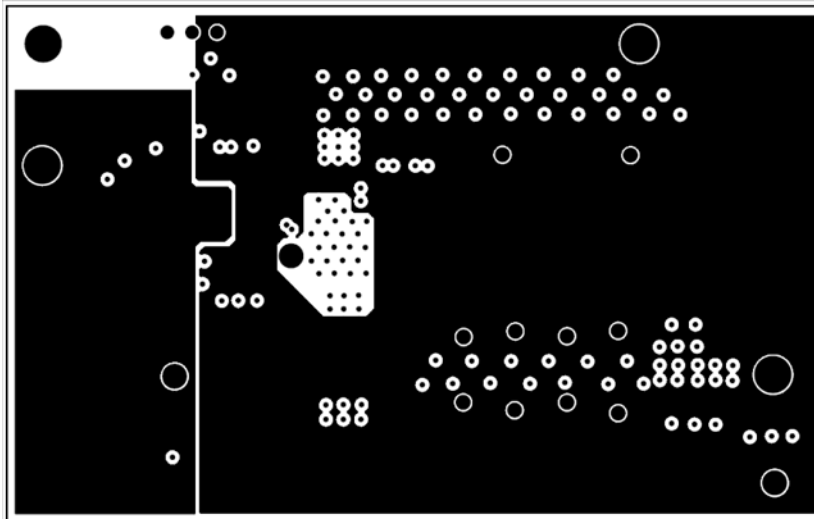


FIGURE 13. LAYER 2

ISL8107EVAL2Z Layout (Continued)

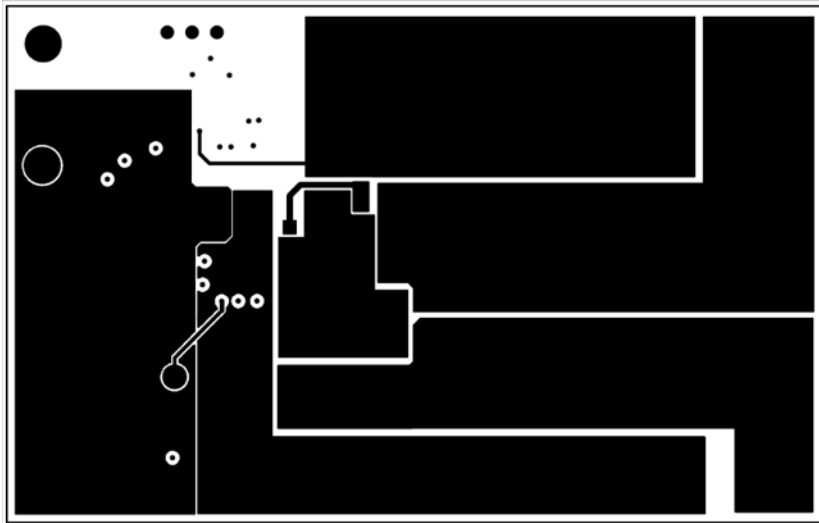


FIGURE 14. LAYER 3

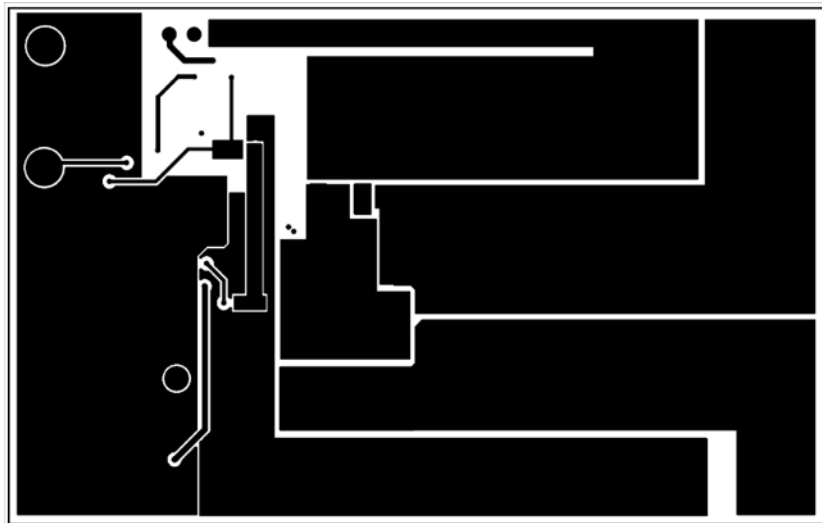


FIGURE 15. BOTTOM LAYER



ISL8107EVAL2Z Layout (Continued)

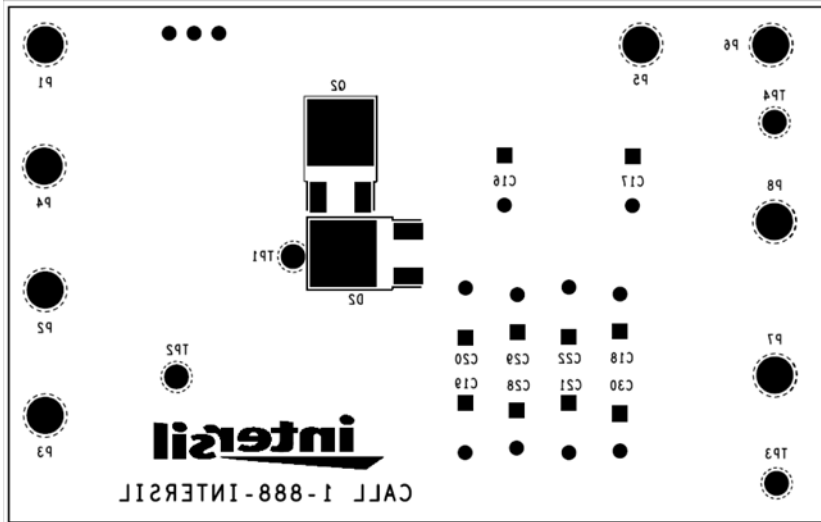


FIGURE 16. BOTTOM SILK SCREEN

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